AK

Notice of Allowability	Application No.	Applicant(s)	
	10/708,586	NOWAK, EDWARD J.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the 07-18-2005 Amendment*.

2. ☒ The allowed claim(s) is/are *1,3-5,7,8,10-12 and 14*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20050930* .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Shouxiang Hu

SHOUXIANG HU
PRIMARY EXAMINER

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Frederick W. Gibb, III (RN: 37,629) on September 30, 2005.

The application has been amended as follows:

IN THE CLAIMS

1. (Currently Amended) An integrated circuit structure comprising:

a substrate having at least two types of crystalline orientations;

first-type transistors formed on first portions of said substrate having a first type of crystalline orientation;

second-type transistors formed on second portions of said substrate having a second type of crystalline orientation different from the first type of crystalline orientation; and

a straining layer above said first-type transistors and said second-type transistors,

wherein said first portions of said substrate comprise a first layer at a top of said first portions, said first layer having said first type of crystalline orientation and a second layer at a bottom of said first portions, said second layer having said second type of crystalline orientation, and

wherein said second portions of said substrate comprise said second layer at a bottom of said second portions and a third layer at a top of said second portions, said third layer

having said second type of crystalline orientation and said third layer contacting said second layer;

wherein said first-type transistors and said second-type transistors include silicide regions and said straining layer is above said silicide regions; and,

wherein said integrated circuit structure further comprises an insulator layer separating said first layer from said second layer.

2. (Canceled)

3. (Previously Presented) The structure in claim ~~2~~ 1, wherein each of said first-type transistors and said second-type transistors include source and drain regions formed within said substrate and a gate conductor formed over said substrate between said source and drain regions, and

wherein said silicide regions are formed over said gate conductor and said source and drain regions.

4. (Original) The structure in claim 1, wherein said first-type transistors are complementary to said second-type transistors.

5. (Original) The structure in claim 1, wherein said ~~first~~ second portions of said substrate comprise non-floating substrate portions and said ~~second~~ first portions of said substrate comprise floating substrate portions.

6. (Canceled).

7. (Original) The structure in claim 1, wherein said first-type transistors and said second-type transistors comprise one of planar complementary metal oxide semiconductor (CMOS) transistors and fin-type field effect transistors (FinFETs).

8. (Currently Amended) An integrated circuit structure comprising:

a substrate having at least two types of crystalline orientations;

N-type field effect transistors (NFETs) formed on first portions of said substrate having a first type of crystalline orientation;

P-type field effect transistors (PFETs) formed on second portions of said substrate having a second type of crystalline orientation different from the first type of crystalline orientation; and

a straining layer above said NFETs and said PFETs,

wherein one of said first portions and said second portions of said substrate comprise a first layer at a top, said first layer having said first type of crystalline orientation and a second layer at a bottom, said second layer having said second type of crystalline orientation, and

wherein the other of said first portions and said second portions of said substrate comprise said second layer at a bottom and a third layer at a top, said third layer having said second type of crystalline orientation and said third layer contacting said second layer;

wherein said NFETs and said PFETs include silicide regions and said straining layer is above said silicide regions; and,

wherein said integrated circuit structure further comprises an insulator layer separating said first layer from said second layer.

9. (Canceled)

10. (Previously Amended) The structure in claim 9 8, wherein each of said NFETs and said PFETs include source and drain regions formed within said substrate and a gate conductor formed over said substrate between said source and drain regions, and

wherein said silicide regions are formed over said gate conductor and said source and drain regions.

11. (Original) The structure in claim 8, wherein said NFETs are complementary to said PFETs.

12. (Original) The structure in claim 8, wherein one of said first portions and said second portions of said substrate comprise non-floating substrate portions and the other of said first portions and said second portions of said substrate comprise floating substrate portions.

13. (Canceled).

14. (Original) The structure in claim 8, wherein said NFETs and said PFETs comprise one of planar complementary metal oxide semiconductor (CMOS) transistors and fin-type field effect transistors (FinFETs).

15-28. (Canceled).

Allowable Subject Matter

Claims 1, 3-5, 7, 8, 10-12 and 14 are allowed.

Drawings

The replacement drawings were received on July 18, 2005. These drawings are approved.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
September 30, 2005

SHOUXIANG HU
PRIMARY EXAMINER